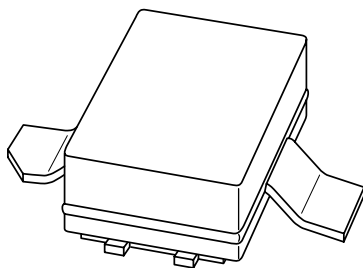


DATA SHEET



BLF1043 UHF power LDMOS transistor

Product specification
Supersedes data of 2002 November 11

2003 Mar 13

UHF power LDMOS transistor

BLF1043

FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 85 mA
 - Output power = 10 W (PEP)
 - Gain = 18.5 dB
 - Efficiency = 40%
 - $d_{im} = -31$ dBc
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (HF to 1 000 MHz)
- No internal matching for broadband operation
- SMD package.

APPLICATIONS

- RF power amplifiers for GSM, EDGE and CDMA base stations and multicarrier applications in the 800 to 1 000 MHz frequency range
- Broadcast drivers.

DESCRIPTION

10 W LDMOS power transistor for base station applications at frequencies from HF to 1 000 MHz.

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, 2-tone, class-AB	$f_1 = 960; f_2 = 960.1$	26	85	10 (PEP)	18.5	40	≤ -31
CW, 1-tone, class-AB	$f = 960$	26	85	10	18.5	52	–

PINNING - SOT538A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

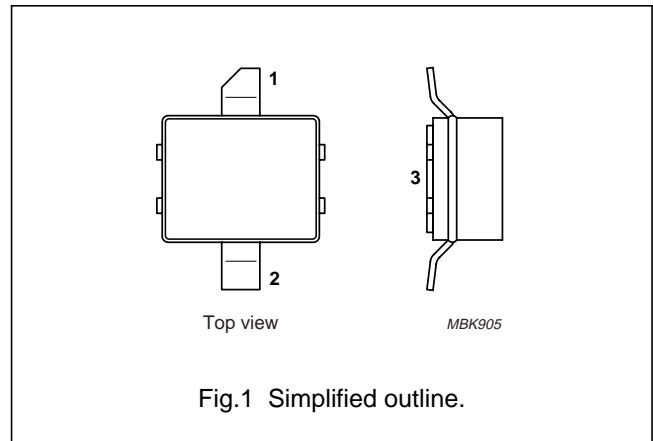


Fig.1 Simplified outline.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	± 15	V
I_D	drain current (DC)	–	2.2	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-h}$	thermal resistance from junction to heatsink	$T_{mb} = 25\text{ °C}$; note 1	9	K/W

Note

1. Thermal resistance is determined under RF operating conditions. Typical value with device soldered on PC board with 32 via holes (diameter 0.3 mm) and thermal compound between PCB and heatsink.

CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.2\text{ mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 20\text{ mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$	–	–	1.5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GSth} + 9\text{ V}$; $V_{DS} = 10\text{ V}$	2.8	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0$	–	–	40	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 0.75\text{ A}$	–	0.5	–	S
R_{DSon}	drain-source on-state resistance	$V_{DS} = 10\text{ V}$; $I_D = 0.75\text{ A}$	–	1.05	–	Ω
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$; $f = 1\text{ MHz}$	–	11	–	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$; $f = 1\text{ MHz}$	–	9	–	pF
C_{rss}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26\text{ V}$; $f = 1\text{ MHz}$	–	0.5	–	pF

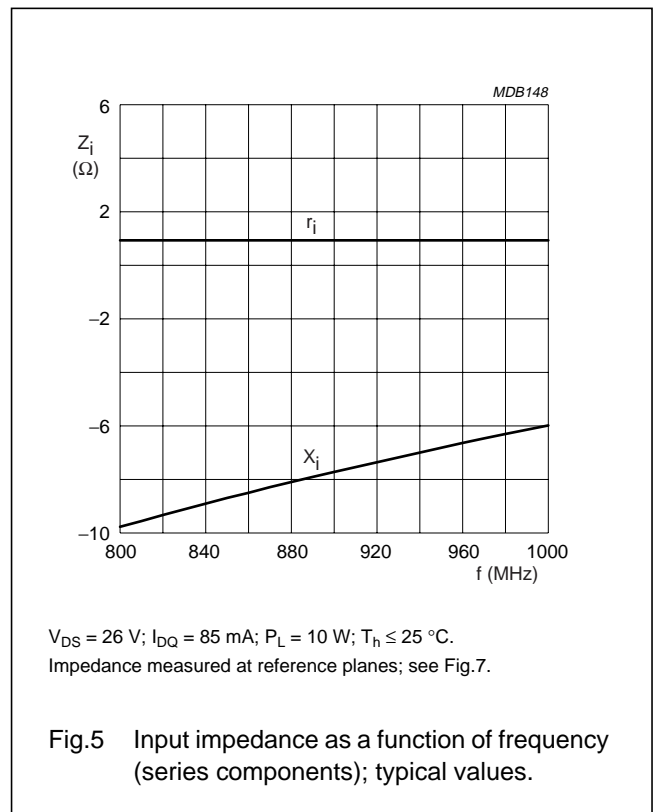
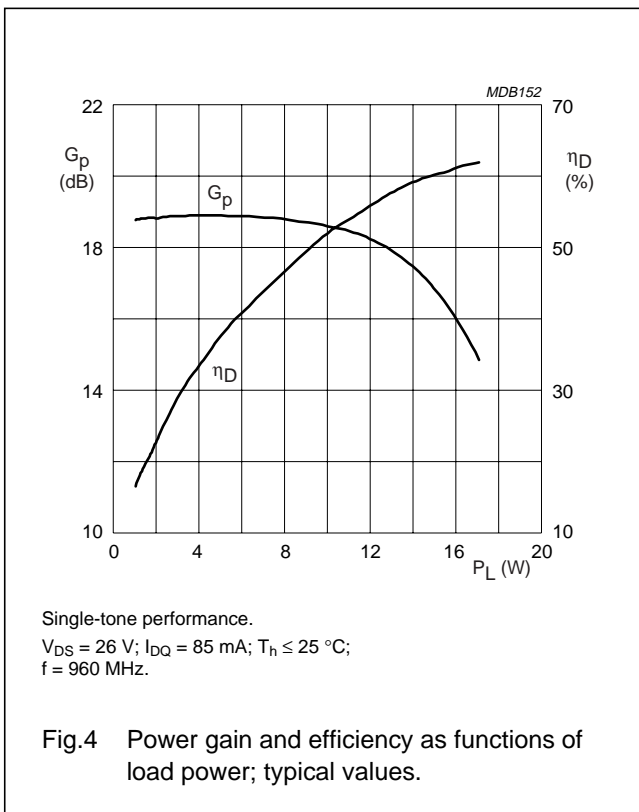
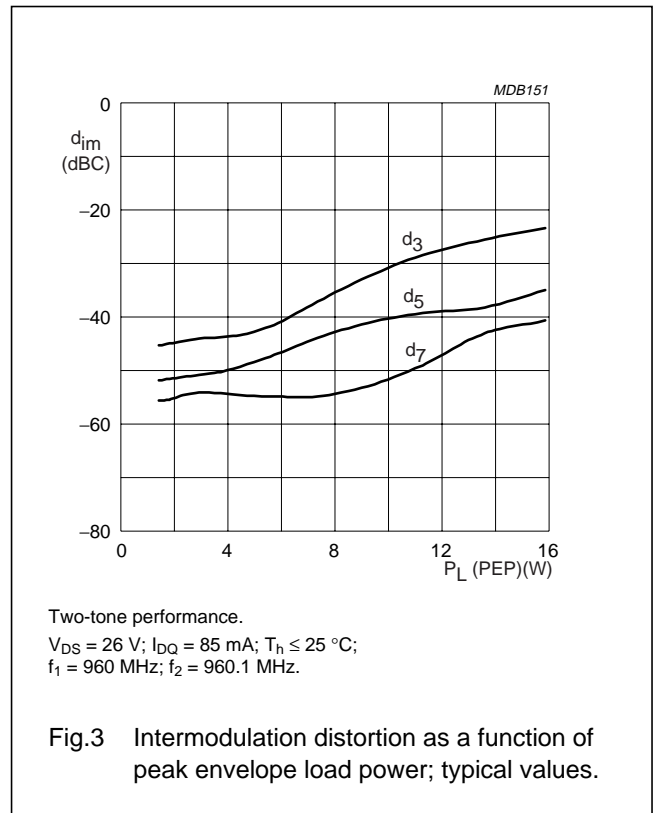
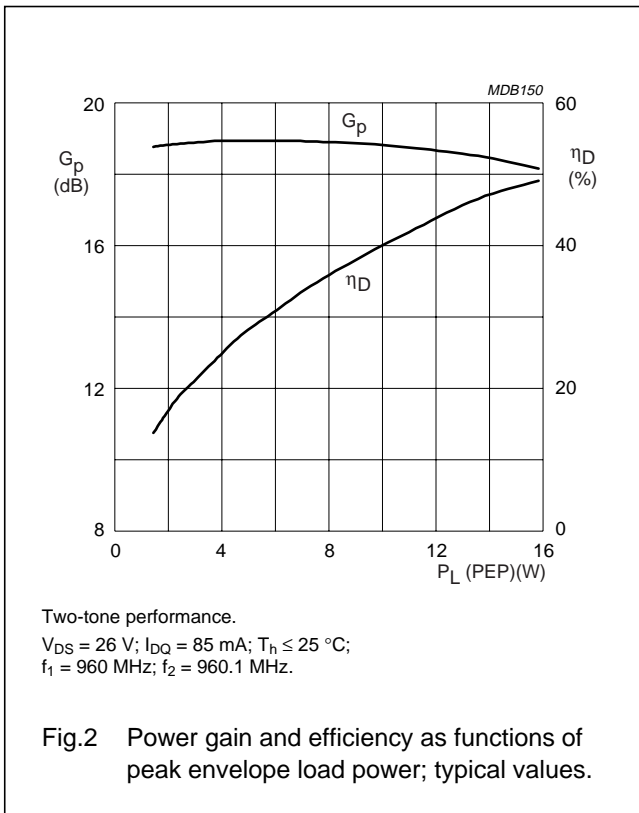
APPLICATION INFORMATIONRF performance in a common source class-AB circuit. $T_h = 25\text{ °C}$; $R_{th\ j-h} = 9\text{ K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, 2-tone, class-AB	$f_1 = 960$; $f_2 = 960.1$	26	85	10 (PEP)	>16.5	>38	≤ -25

Ruggedness in class-AB operationThe BLF1043 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 26\text{ V}$; $f = 960\text{ MHz}$ at rated load power.

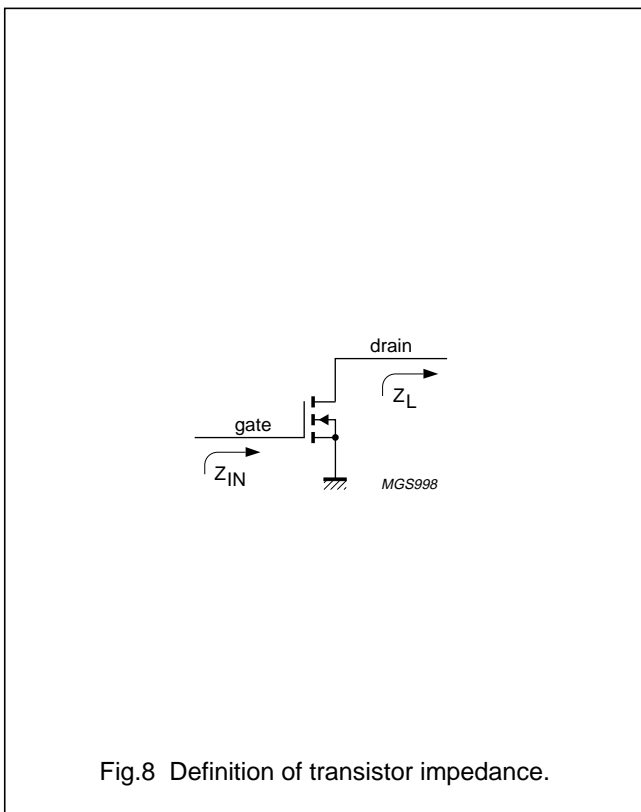
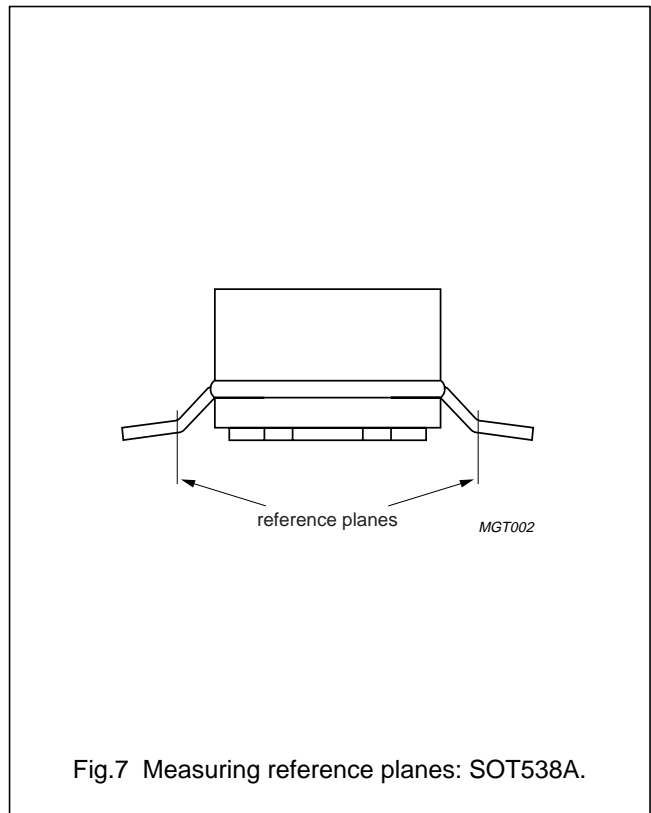
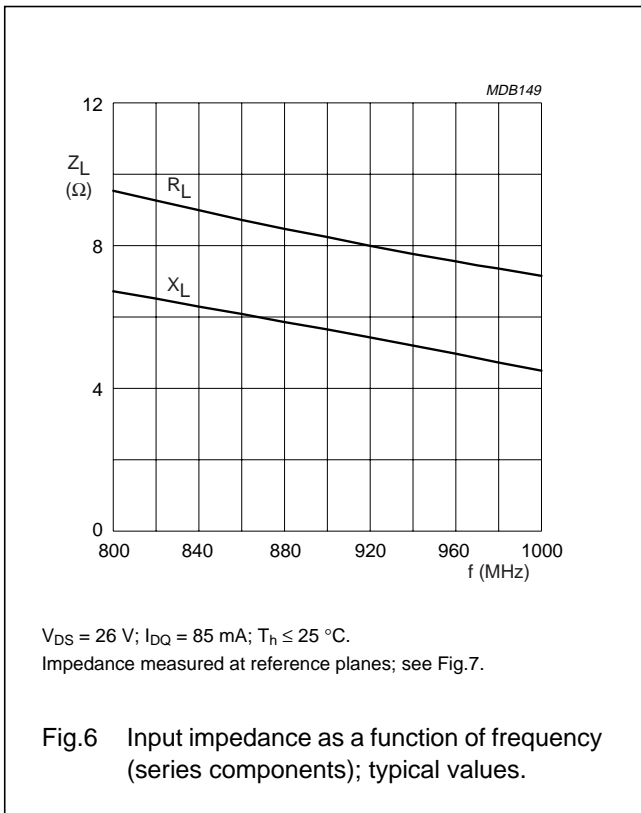
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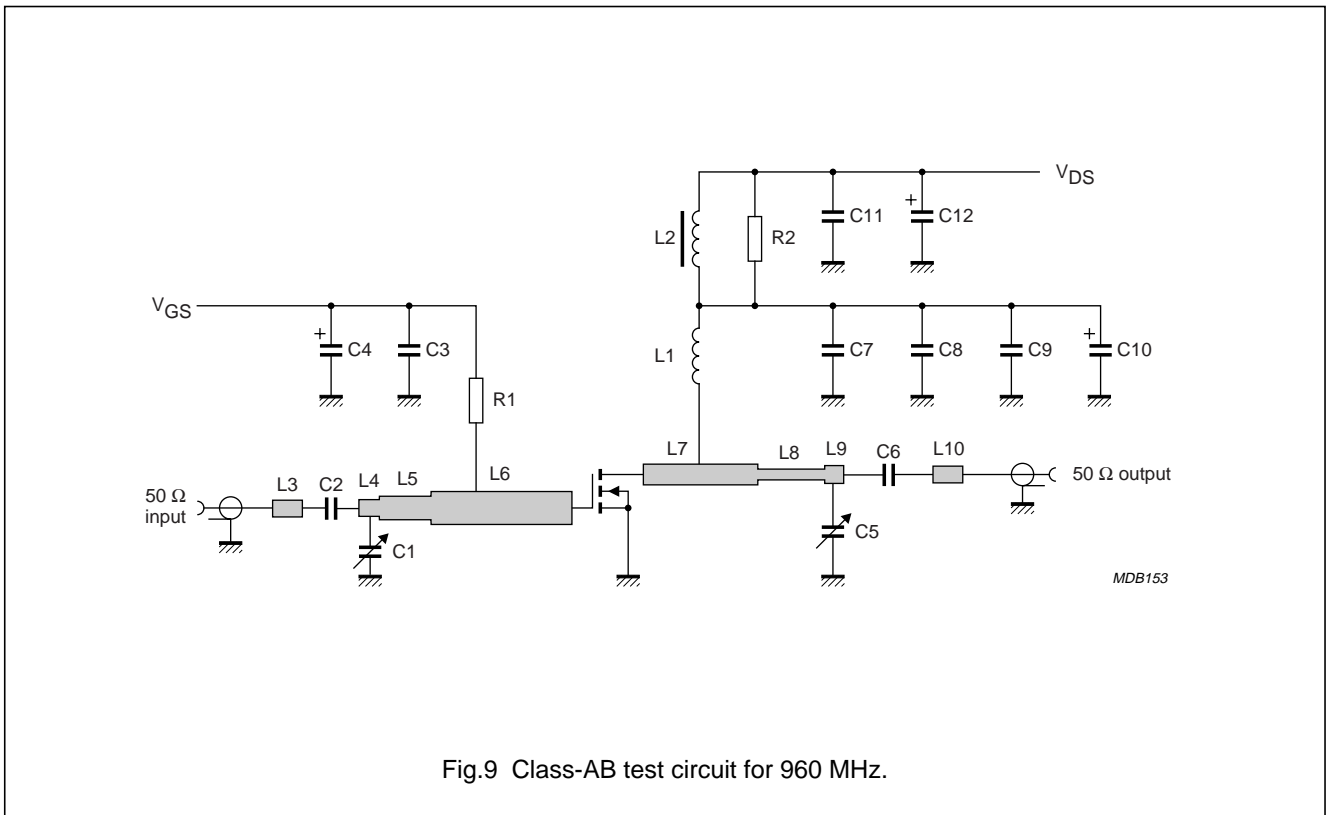


Fig.9 Class-AB test circuit for 960 MHz.

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List of components (see Figs 9 and 10)

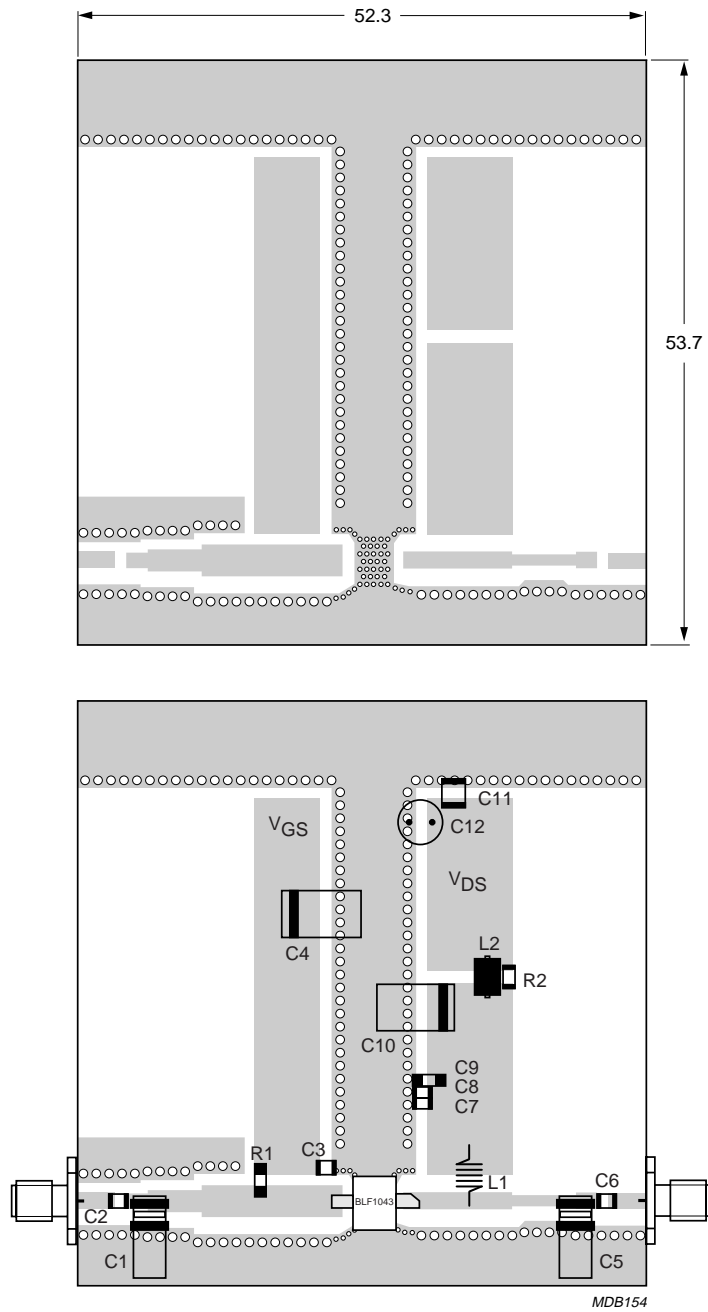
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C5	Tekelec variable capacitor	0.8 to 8 pF		
C2, C3, C6, C7	multilayer ceramic chip capacitor; note 1	56 pF		
C4, C10	tantalum SMD capacitor	10 μ F; 35 V		
C8	multilayer ceramic chip capacitor; note 1	1 nF		
C9	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C11	multilayer ceramic chip capacitor; note 2	1 nF		
C12	electrolytic capacitor	100 μ F; 63 V		2222 037 58101
L1	3 turns enamelled 0.5 mm copper wire		3 loops; d = 3.5 mm	
L2	ferrite bead; ferroxcube CBD4.6/3/3-4S2			
L3	stripline; note 3	50 Ω	3.5 \times 1.5 mm	
L4	stripline; note 3	50 Ω	2 \times 1.5 mm	
L5	stripline; note 3	42 Ω	5 \times 2 mm	
L6	stripline; note 3	31 Ω	13 \times 3 mm	
L7	stripline; note 3	50 Ω	10 \times 1.5 mm	
L8	stripline; note 3	65 Ω	5.9 \times 1 mm	
L9	stripline; note 3	50 Ω	2 \times 1.5 mm	
L10	stripline; note 3	50 Ω	3.5 \times 1.5 mm	
R1	metal film resistor	39 Ω , 0.6 W		
R2	metal film resistor	10 Ω , 0.6 W		2322 256 11009

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Rogers 5880 dielectric ($\epsilon_r = 2.2$); thickness 0.51 mm.

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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$), thickness 0.51 mm. The other side is unetched and serves as a ground plane.

Fig.10 Component layout for 960 MHz class-AB test circuit.

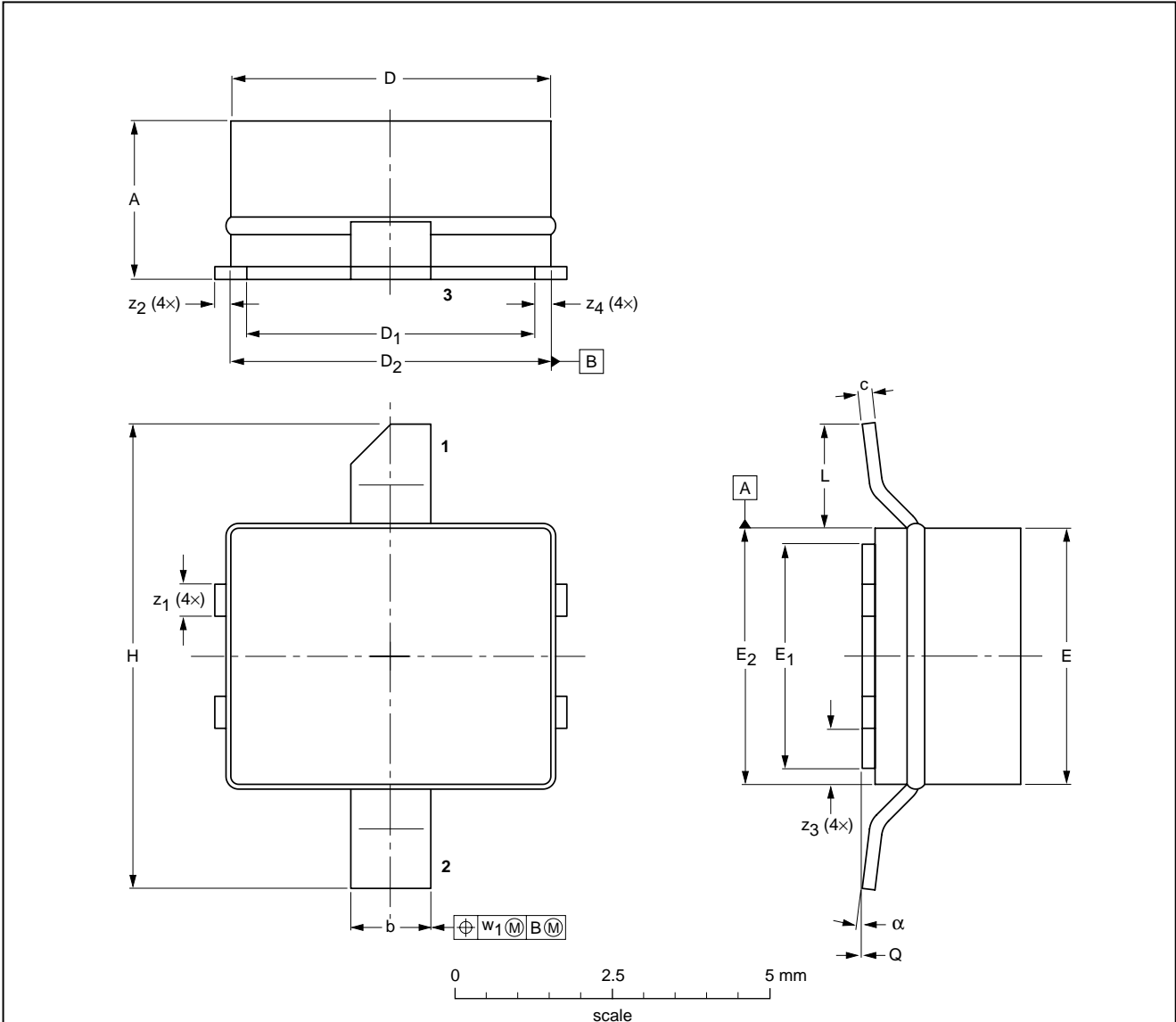
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PACKAGE OUTLINE

Ceramic surface mounted package; 2 leads

SOT538A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	D ₂	E	E ₁	E ₂	H	L	Q	w ₁	z ₁	z ₂	z ₃	z ₄	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.16 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	0.58 0.43	0.25 0.18	0.97 0.81	0.51 0.00	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.203 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	0.023 0.017	0.010 0.007	0.038 0.032	0.020 0.000	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT538A						00-03-03- 02-08-20

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DATA SHEET STATUS

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